FIG. 1

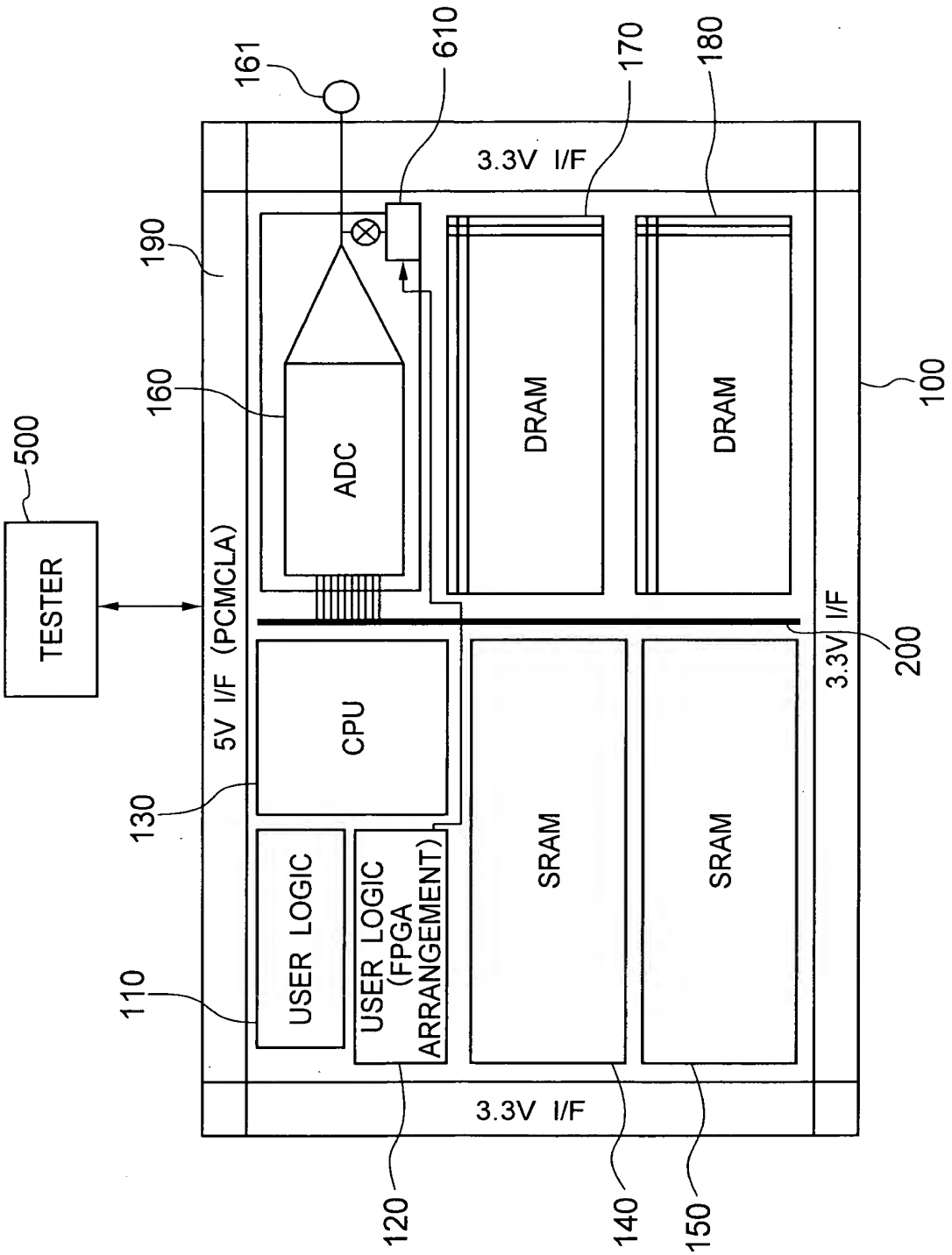

TESTER
500
5V I/F (PCMCLA)
ADC
160
DRAM
DRAM
3.3V I/F
161
610
170
180
190
100
200
3.3V I/F
CPU
130
USER LOGIC
USER LOGIC (FPGA ARRANGEMENT)
110
SRAM
SRAM
3.3V I/F
120
140
150

FIG. 2

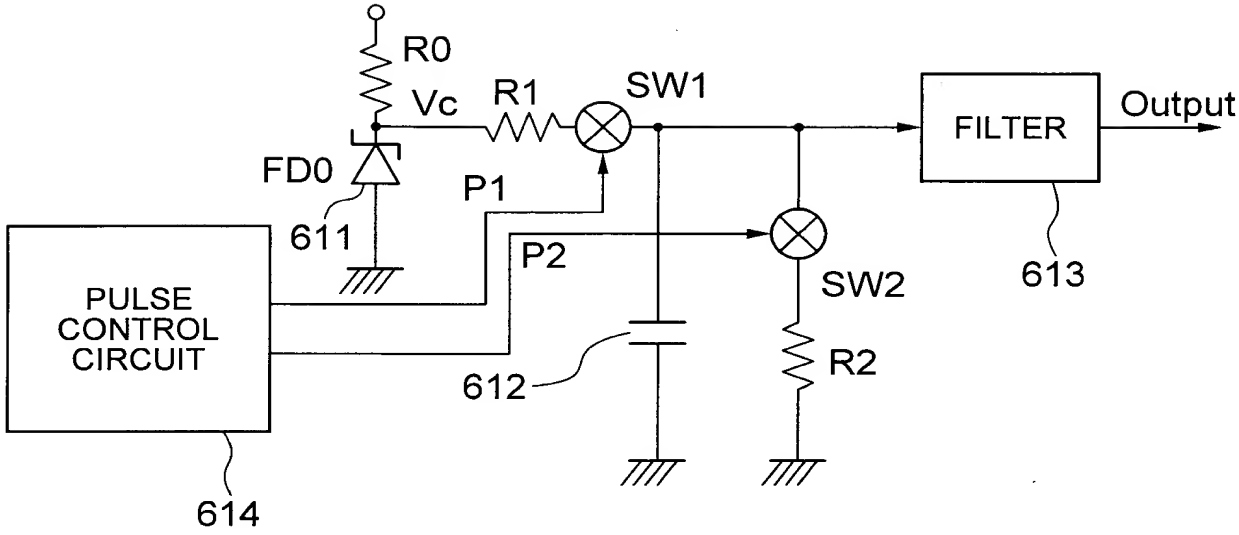

R0
Vc
R1
SW1
FILTER
Output
FD0
P1
611
P2
SW2
613
PULSE
CONTROL
CIRCUIT
612
R2
614

FIG. 3

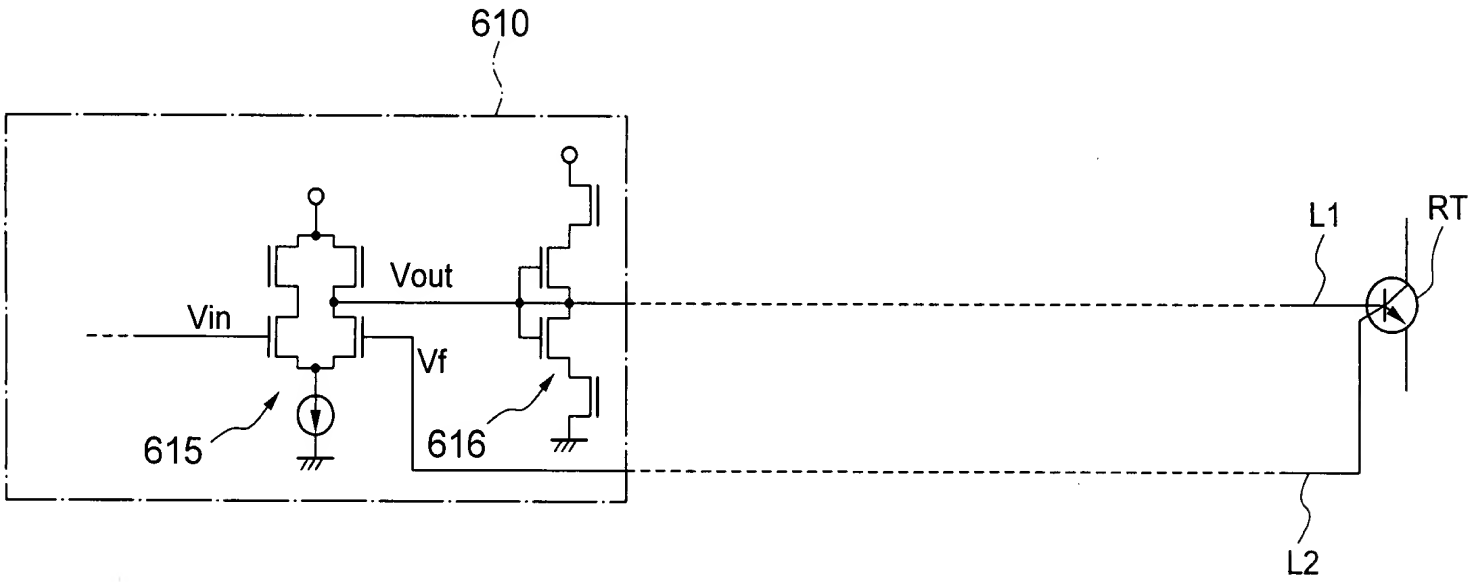
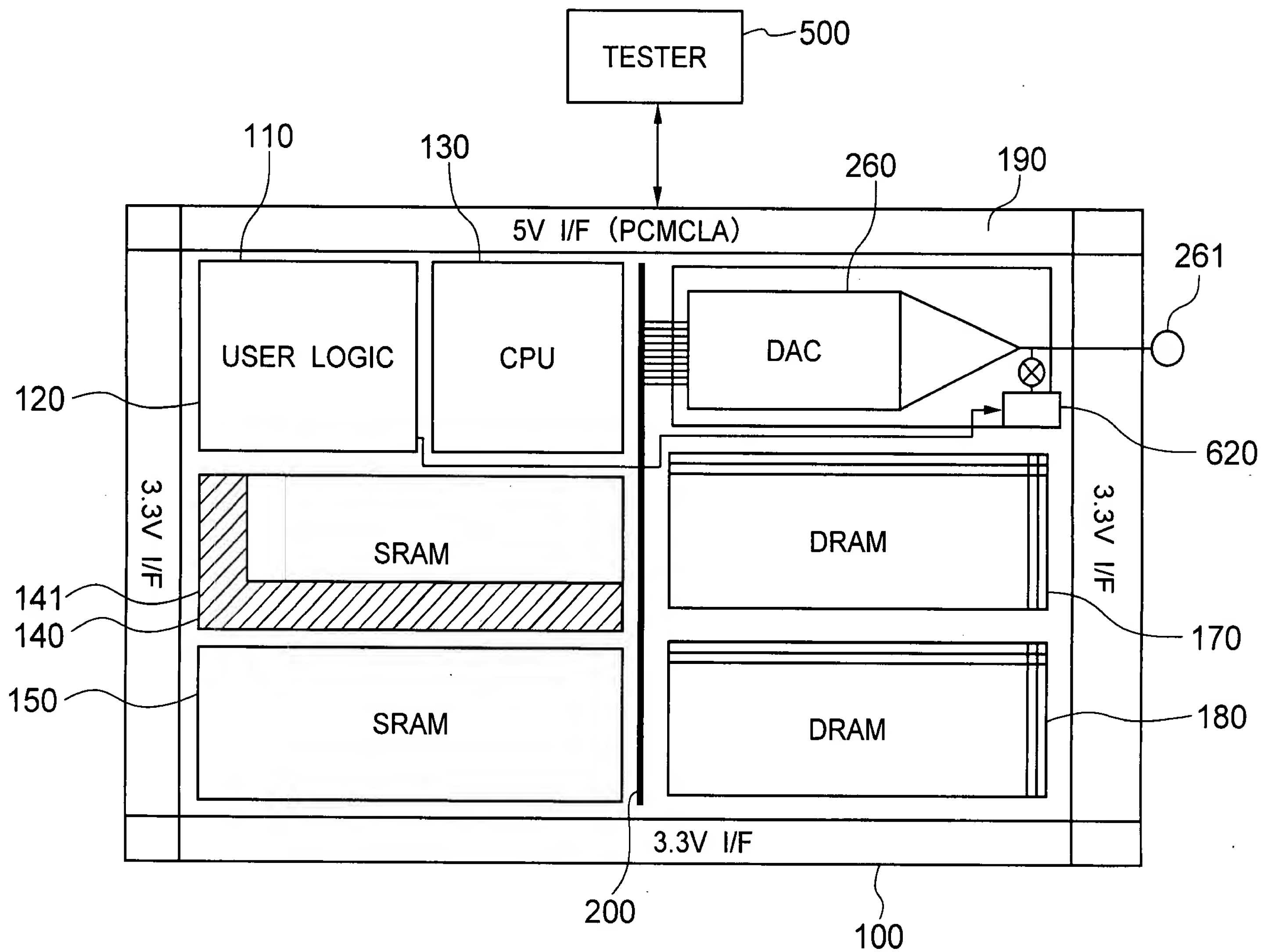


FIG. 4



TESTER
500
110
130
260
190
5V I/F (PCMCLA)
261
USER LOGIC
CPU
DAC
120
620
3.3V I/F
SRAM
DRAM
3.3V I/F
141
140
170
150
SRAM
DRAM
180
3.3V I/F
200
100

FIG. 5

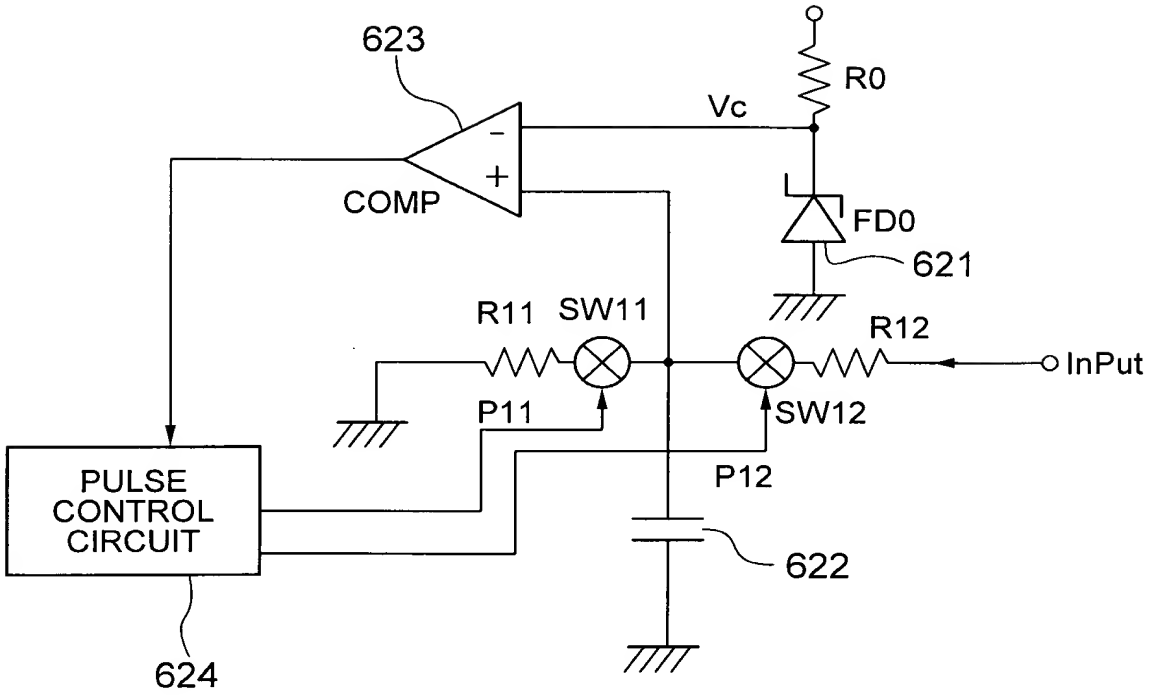

623
R0
Vc
COMP
FD0
621
R11
SW11
R12
InPut
P11
SW12
P12
PULSE
CONTROL
CIRCUIT
622
624

FIG. 6

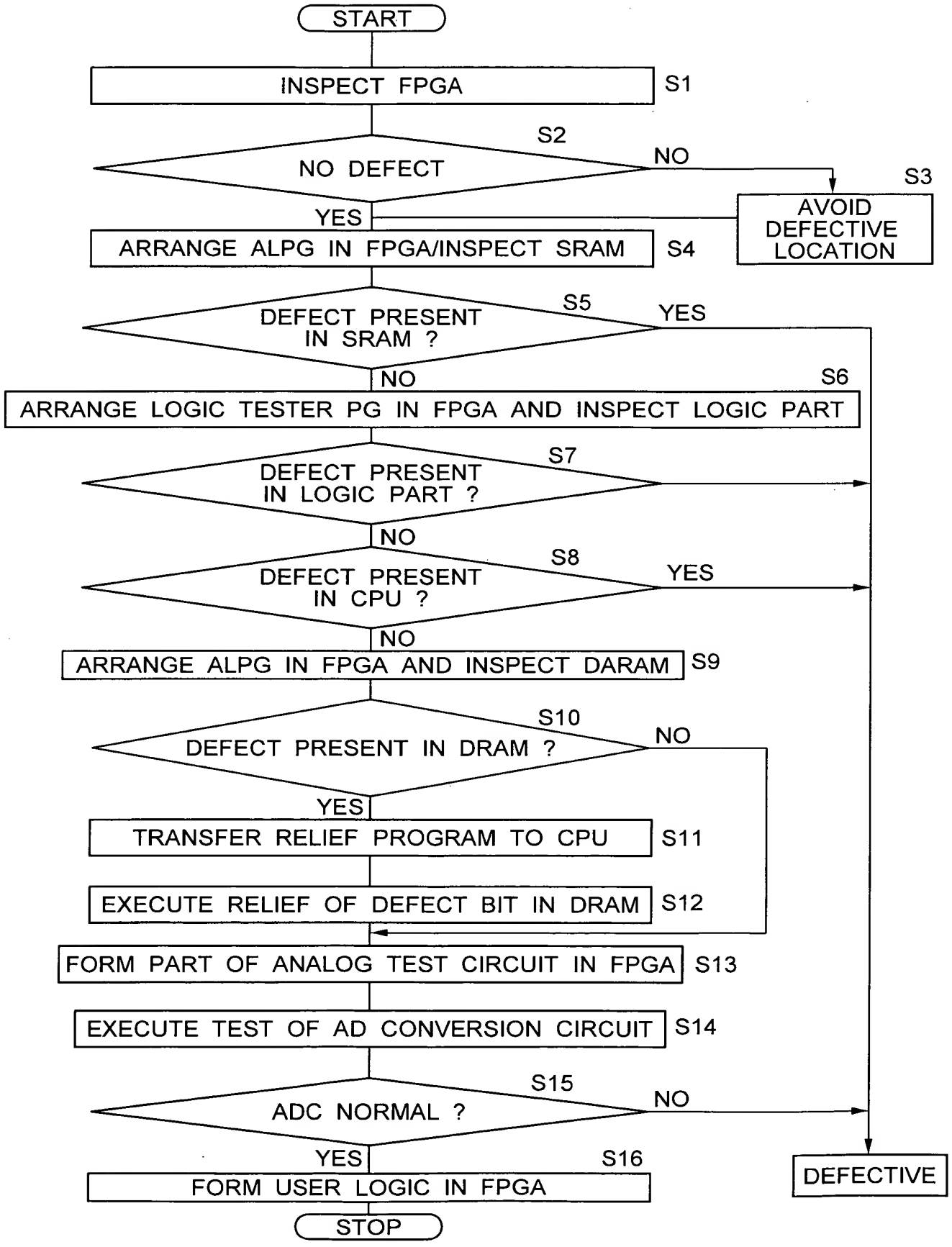
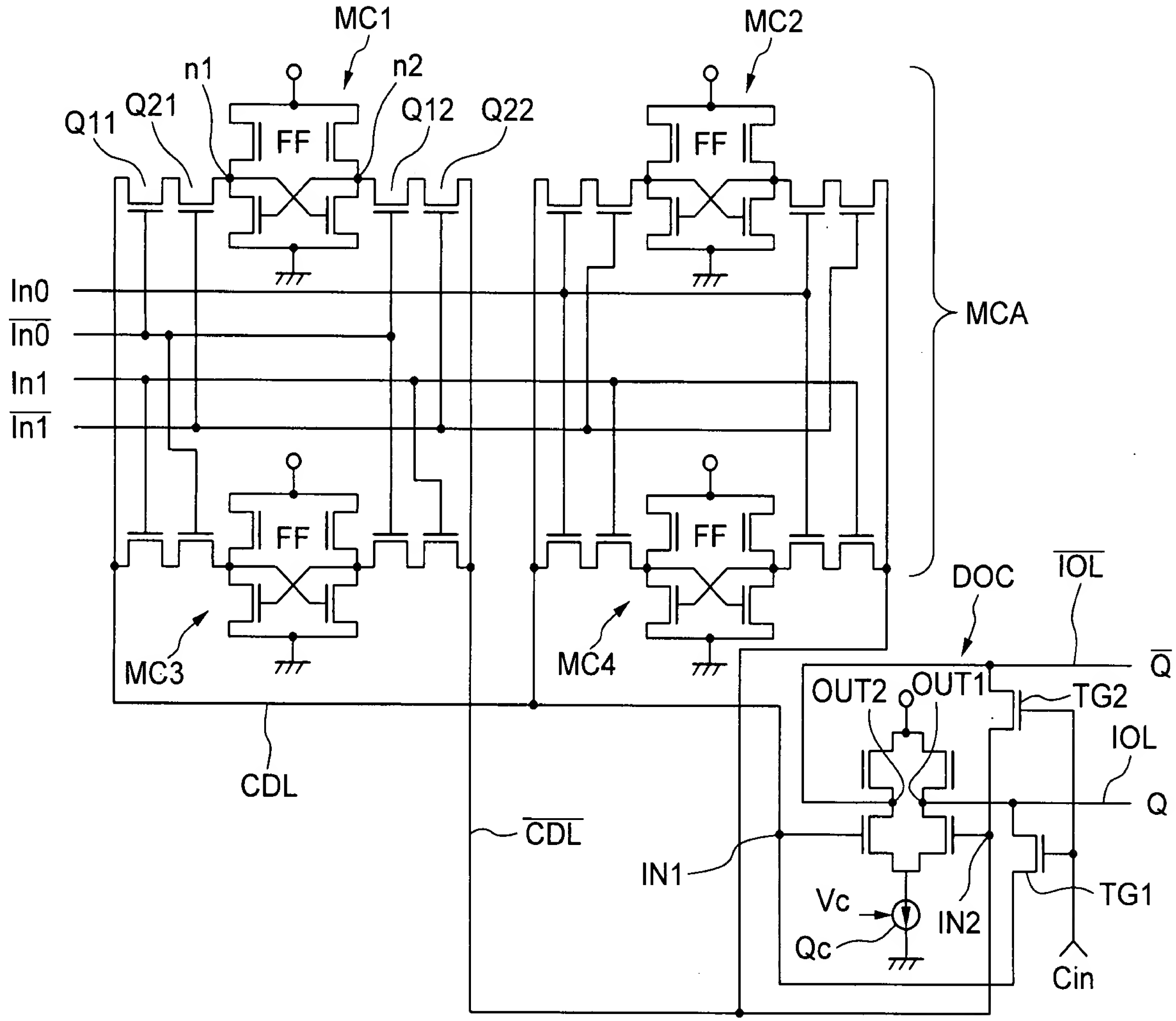

START
INSPECT FPGA
S1
S2
NO DEFECT
NO
S3
AVOID DEFECTIVE LOCATION
YES
ARRANGE ALPG IN FPGA/INSPECT SRAM
S4
S5
DEFECT PRESENT IN SRAM ?
YES
NO
S6
ARRANGE LOGIC TESTER PG IN FPGA AND INSPECT LOGIC PART
S7
DEFECT PRESENT IN LOGIC PART ?
NO
S8
DEFECT PRESENT IN CPU ?
YES
NO
ARRANGE ALPG IN FPGA AND INSPECT DARAM
S9
S10
DEFECT PRESENT IN DRAM ?
NO
YES
TRANSFER RELIEF PROGRAM TO CPU
S11
EXECUTE RELIEF OF DEFECT BIT IN DRAM
S12
FORM PART OF ANALOG TEST CIRCUIT IN FPGA
S13
EXECUTE TEST OF AD CONVERSION CIRCUIT
S14
S15
ADC NORMAL ?
NO
YES
S16
FORM USER LOGIC IN FPGA
STOP
DEFECTIVE

FIG. 7



MC1
MC2
n1
n2
Q11
Q21
Q12
Q22
FF
FF
FF
FF
In0
$\overline{In0}$
In1
$\overline{In1}$
MCA
MC3
MC4
DOC
$\overline{IOL}$
$\overline{Q}$
OUT2
OUT1
TG2
IOL
Q
CDL
$\overline{CDL}$
IN1
IN2
Vc
Qc
TG1
Cin

FIG. 8

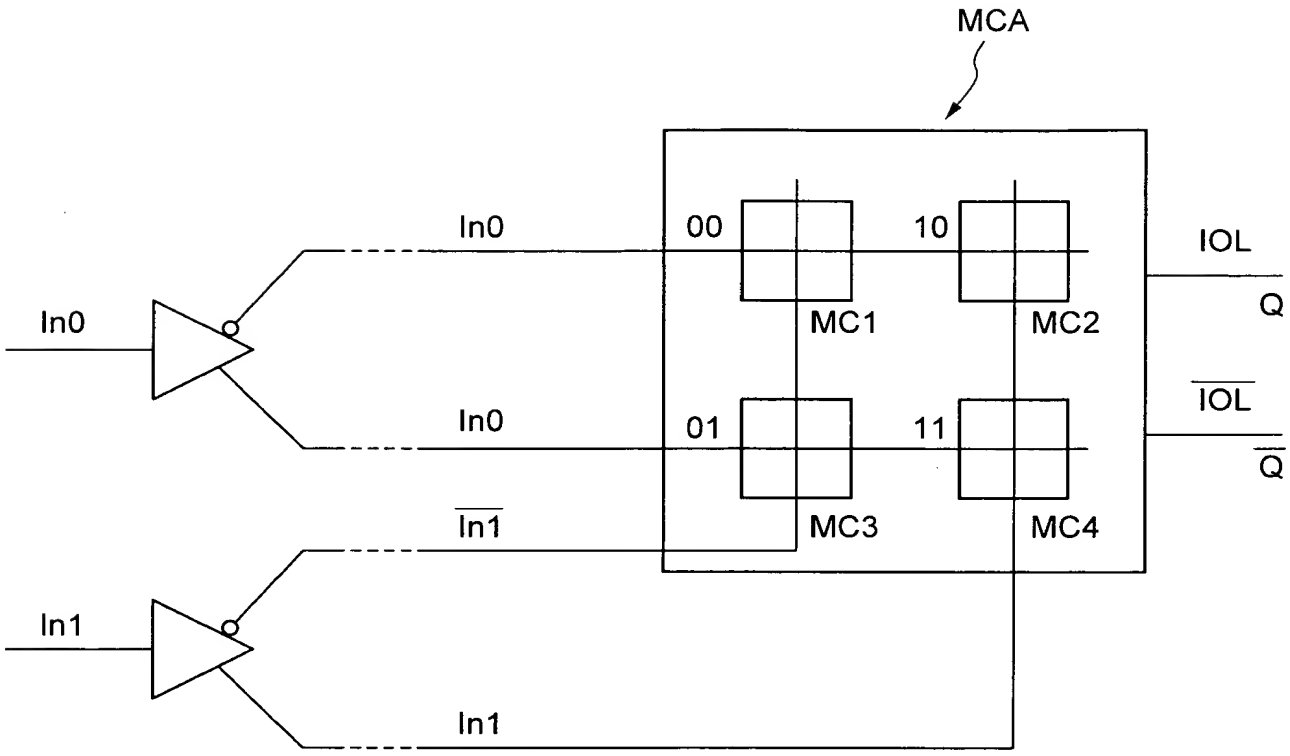


FIG. 9

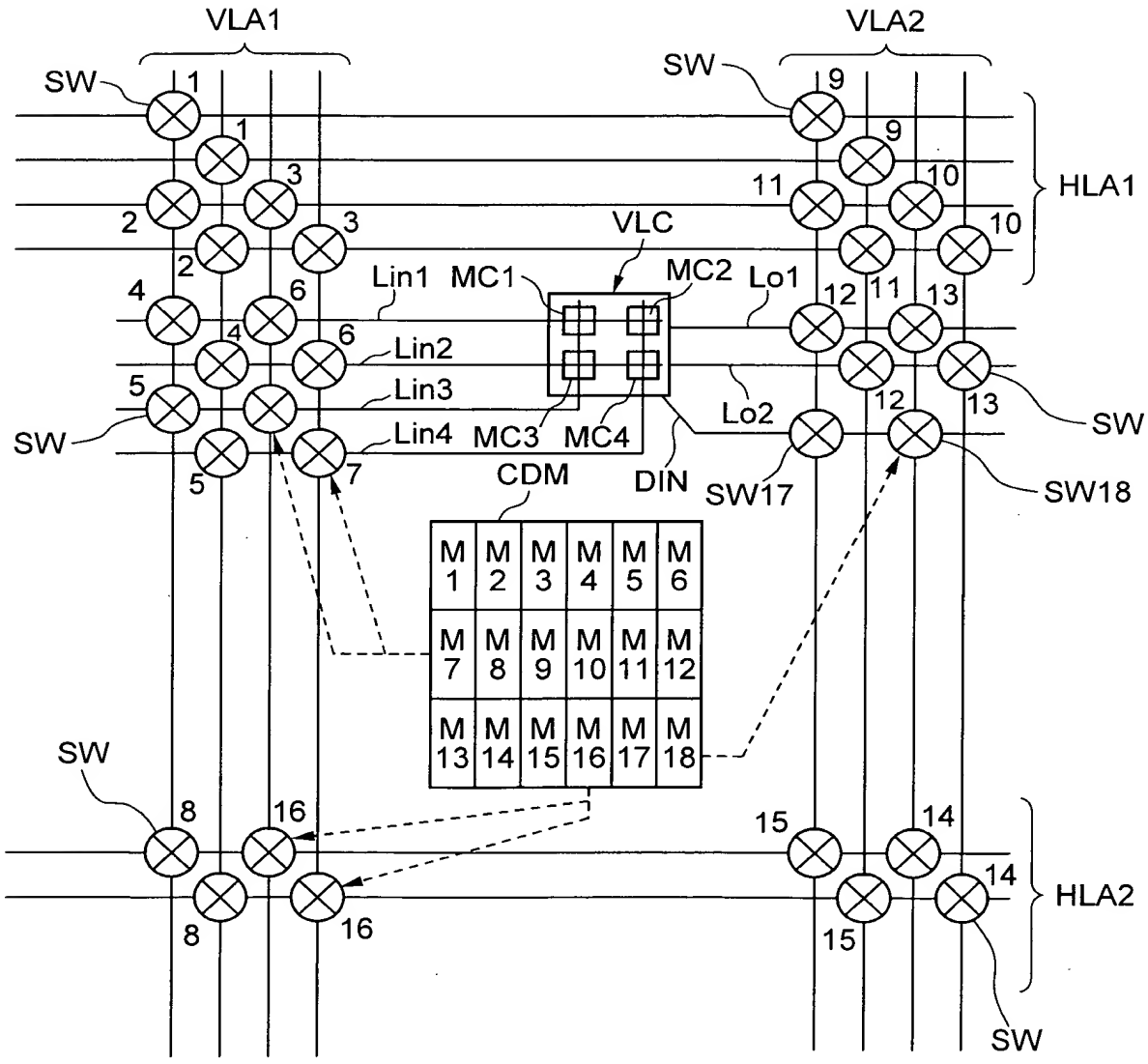

VLA1
VLA2
SW
HLA1
HLA2
VLC
Lin1
MC1
MC2
Lo1
Lin2
Lin3
Lin4
MC3
MC4
Lo2
DIN
SW17
SW18
CDM
M1
M2
M3
M4
M5
M6
M7
M8
M9
M10
M11
M12
M13
M14
M15
M16
M17
M18

FIG. 10

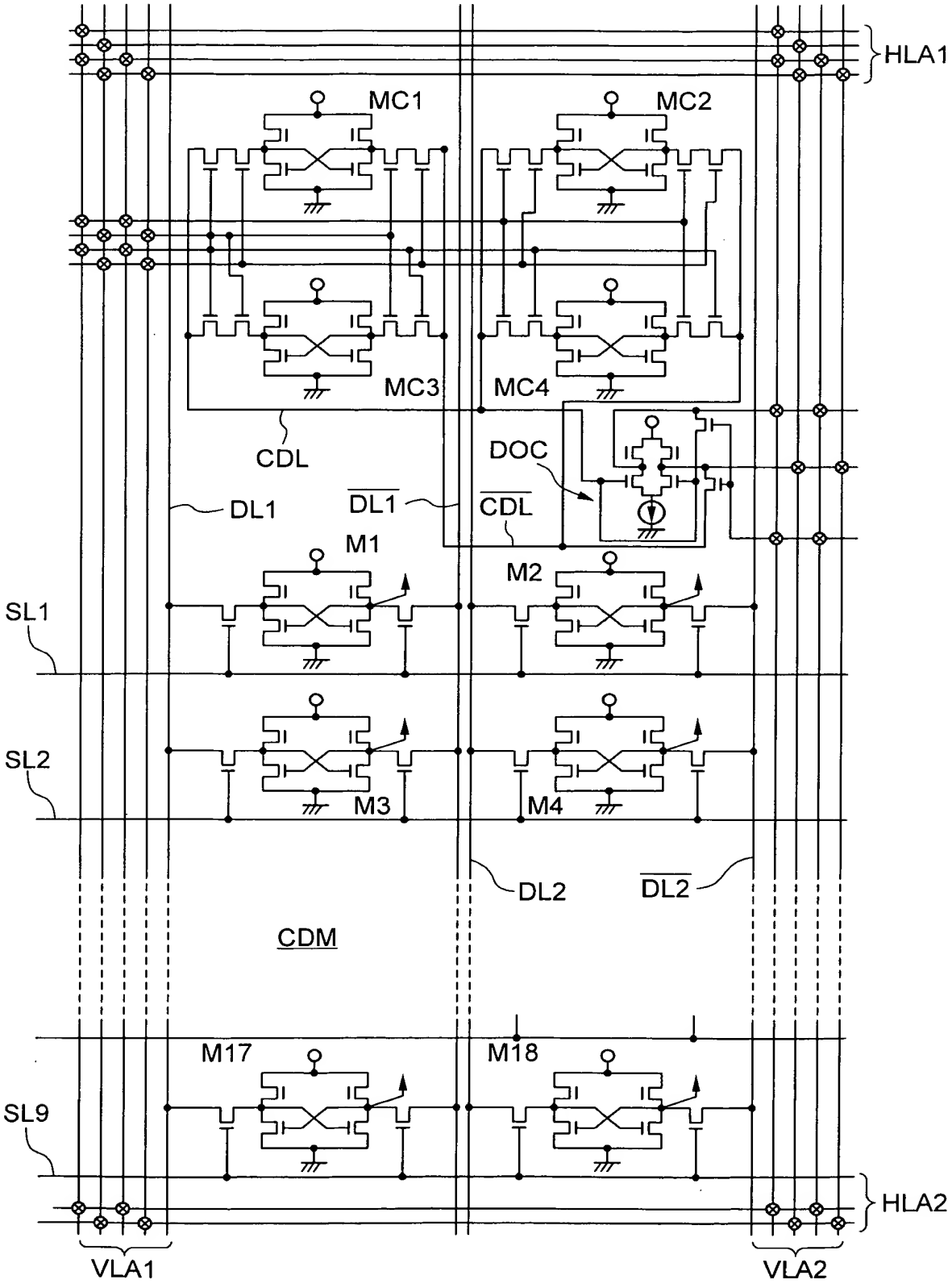

HLA1
MC1
MC2
MC3
MC4
CDL
DOC
DL1
$\overline{DL1}$
$\overline{CDL}$
M1
M2
SL1
SL2
M3
M4
DL2
$\overline{DL2}$
CDM
M17
M18
SL9
HLA2
VLA1
VLA2

FIG. 11

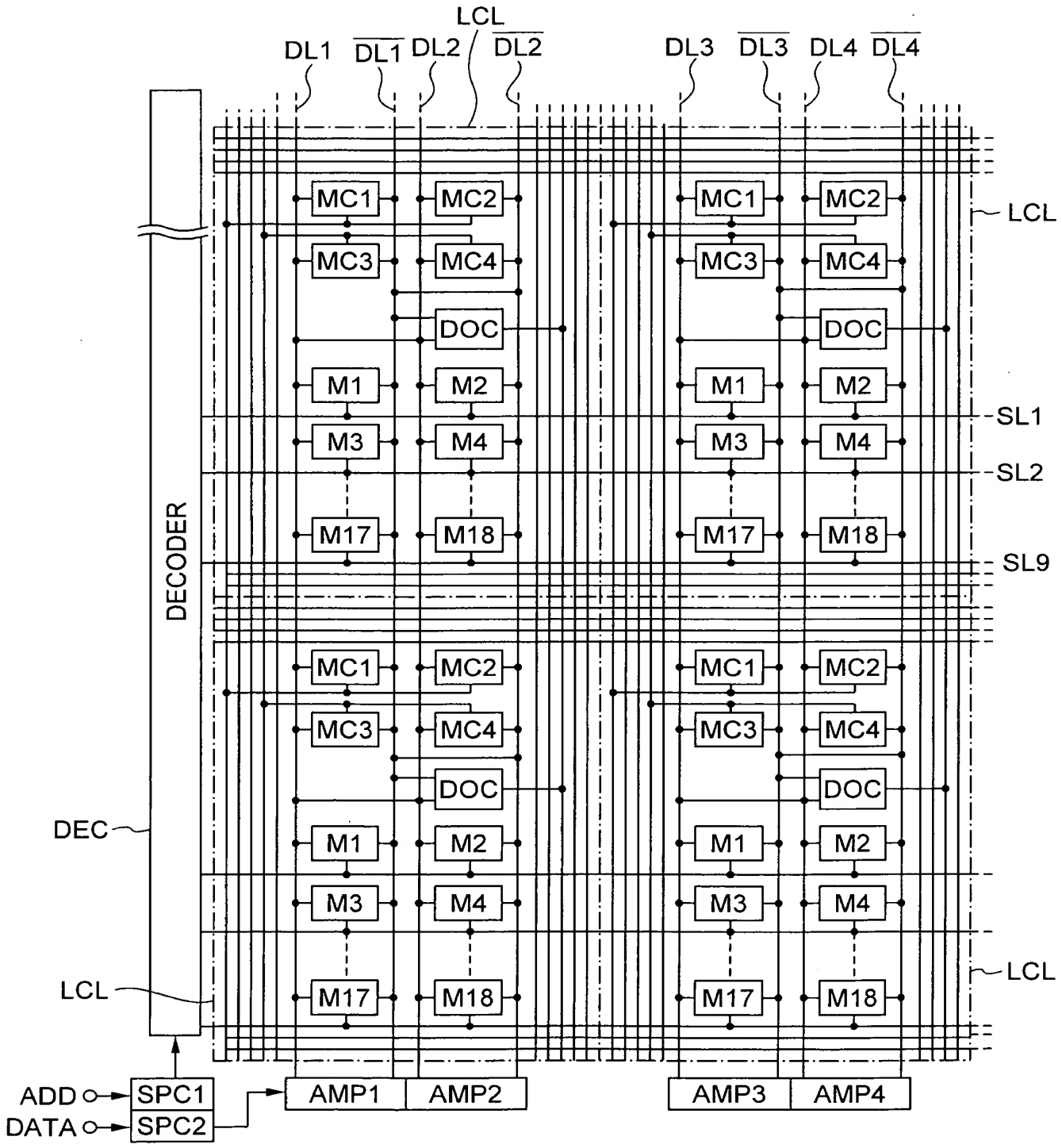

LCL
DL1
DL1
DL2
DL2
DL3
DL3
DL4
DL4
MC1
MC2
MC3
MC4
DOC
M1
M2
M3
M4
M17
M18
LCL
SL1
SL2
SL9
DECODER
DEC
LCL
ADD
DATA
SPC1
SPC2
AMP1
AMP2
AMP3
AMP4

FIG. 12

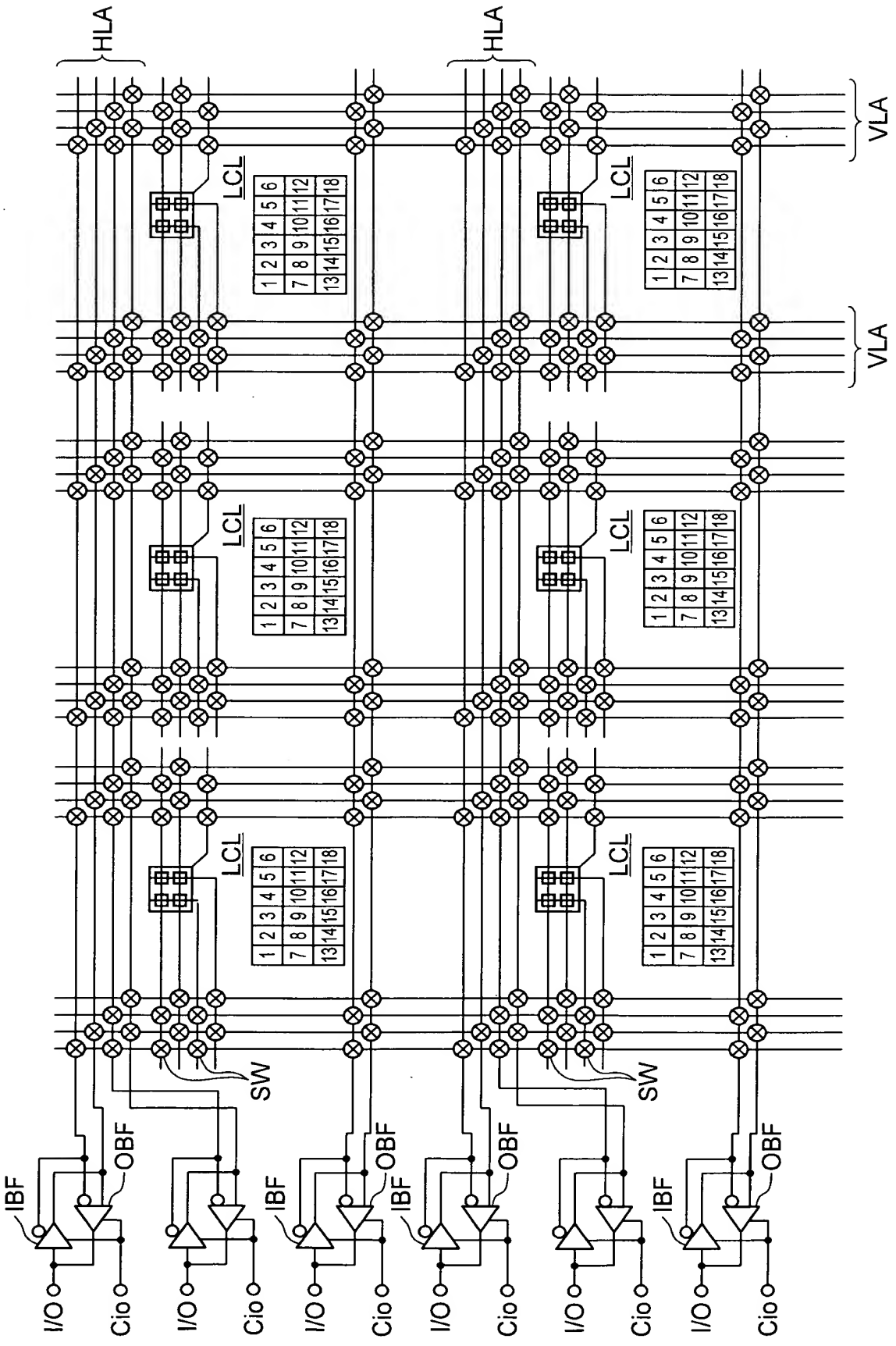


FIG. 13

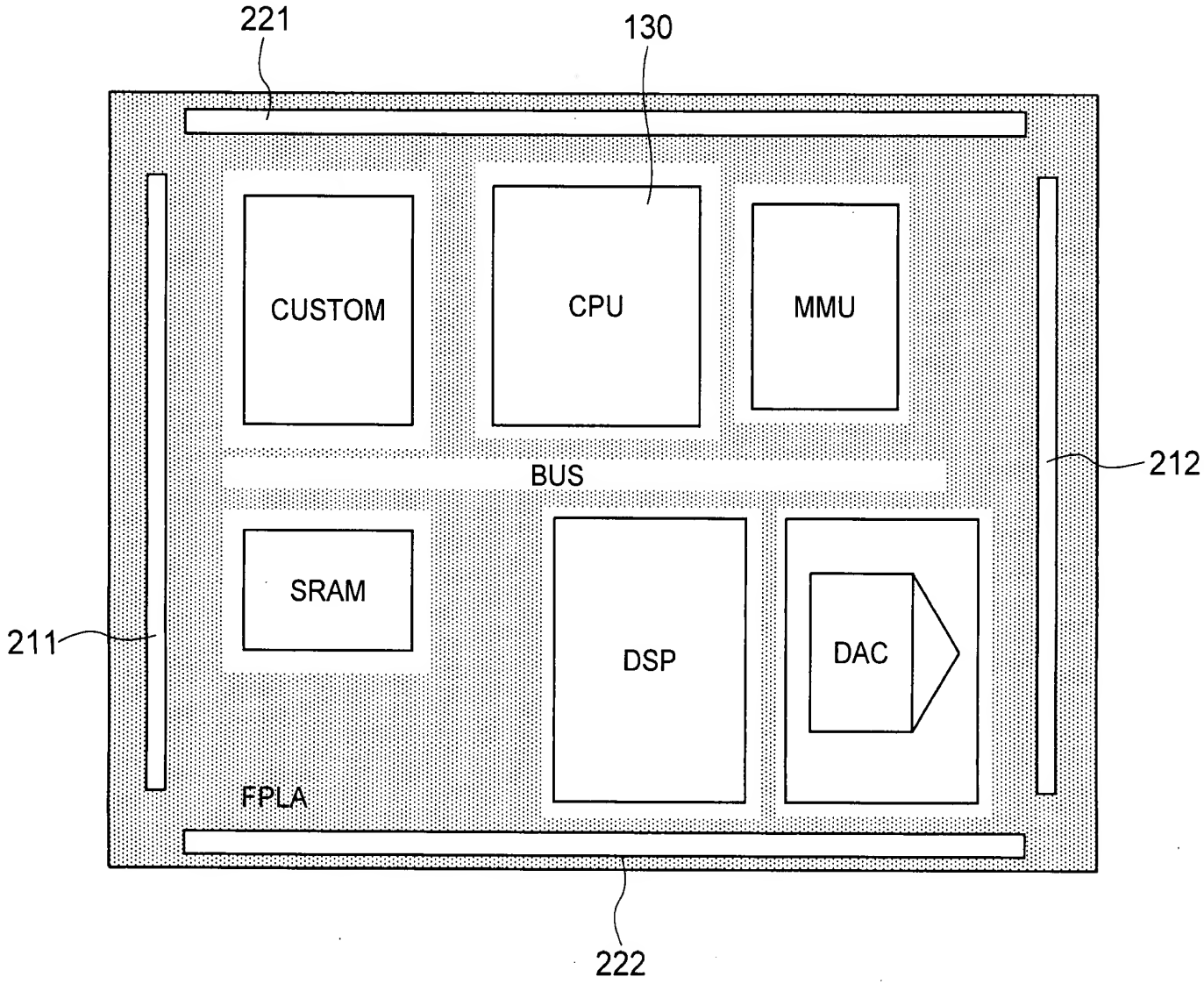


FIG. 14

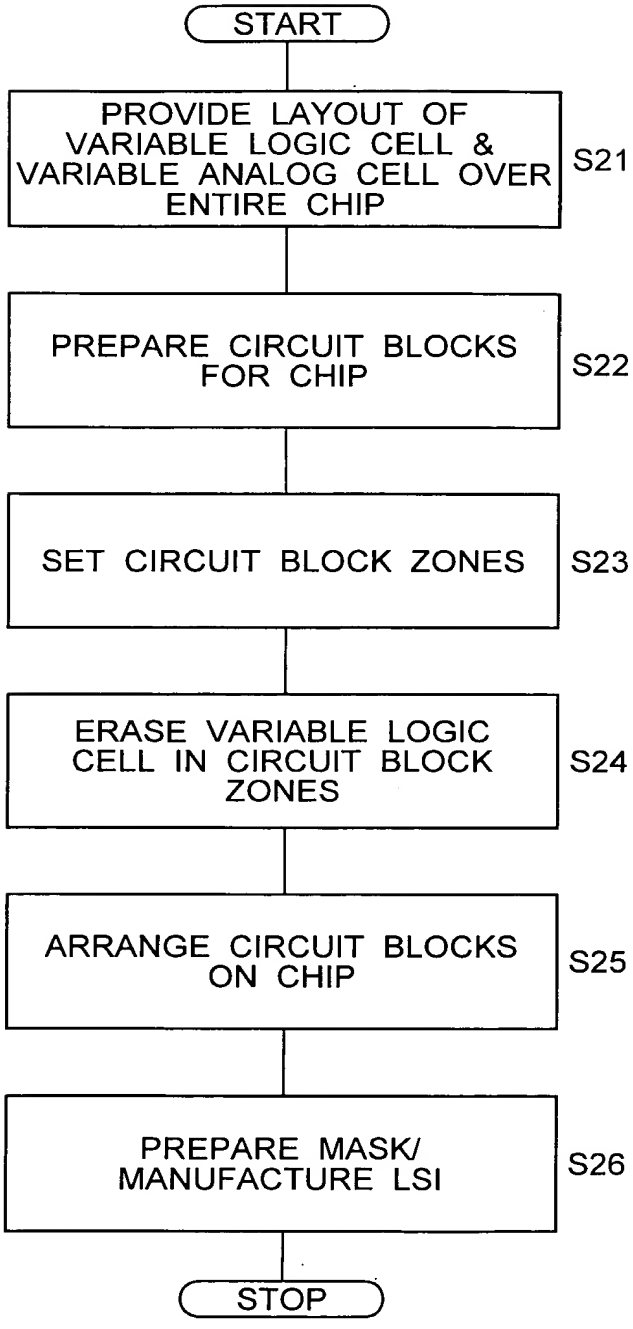

START
PROVIDE LAYOUT OF VARIABLE LOGIC CELL & VARIABLE ANALOG CELL OVER ENTIRE CHIP
S21
PREPARE CIRCUIT BLOCKS FOR CHIP
S22
SET CIRCUIT BLOCK ZONES
S23
ERASE VARIABLE LOGIC CELL IN CIRCUIT BLOCK ZONES
S24
ARRANGE CIRCUIT BLOCKS ON CHIP
S25
PREPARE MASK/ MANUFACTURE LSI
S26
STOP

FIG. 15

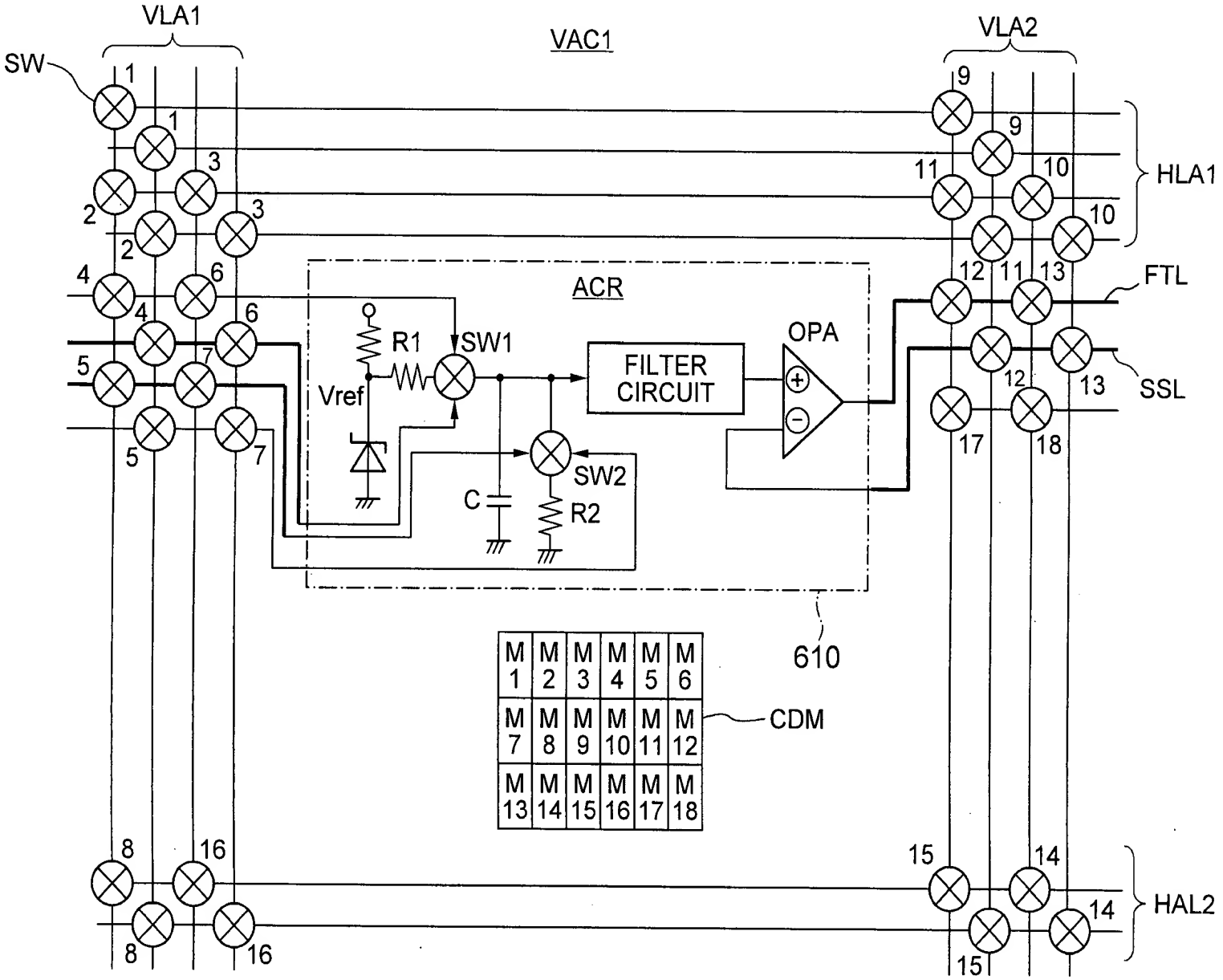

VLA1
VAC1
VLA2
SW
HLA1
FTL
SSL
HAL2
ACR
R1
SW1
Vref
FILTER CIRCUIT
OPA
SW2
C
R2
610
CDM
M1 M2 M3 M4 M5 M6
M7 M8 M9 M10 M11 M12
M13 M14 M15 M16 M17 M18

FIG. 16

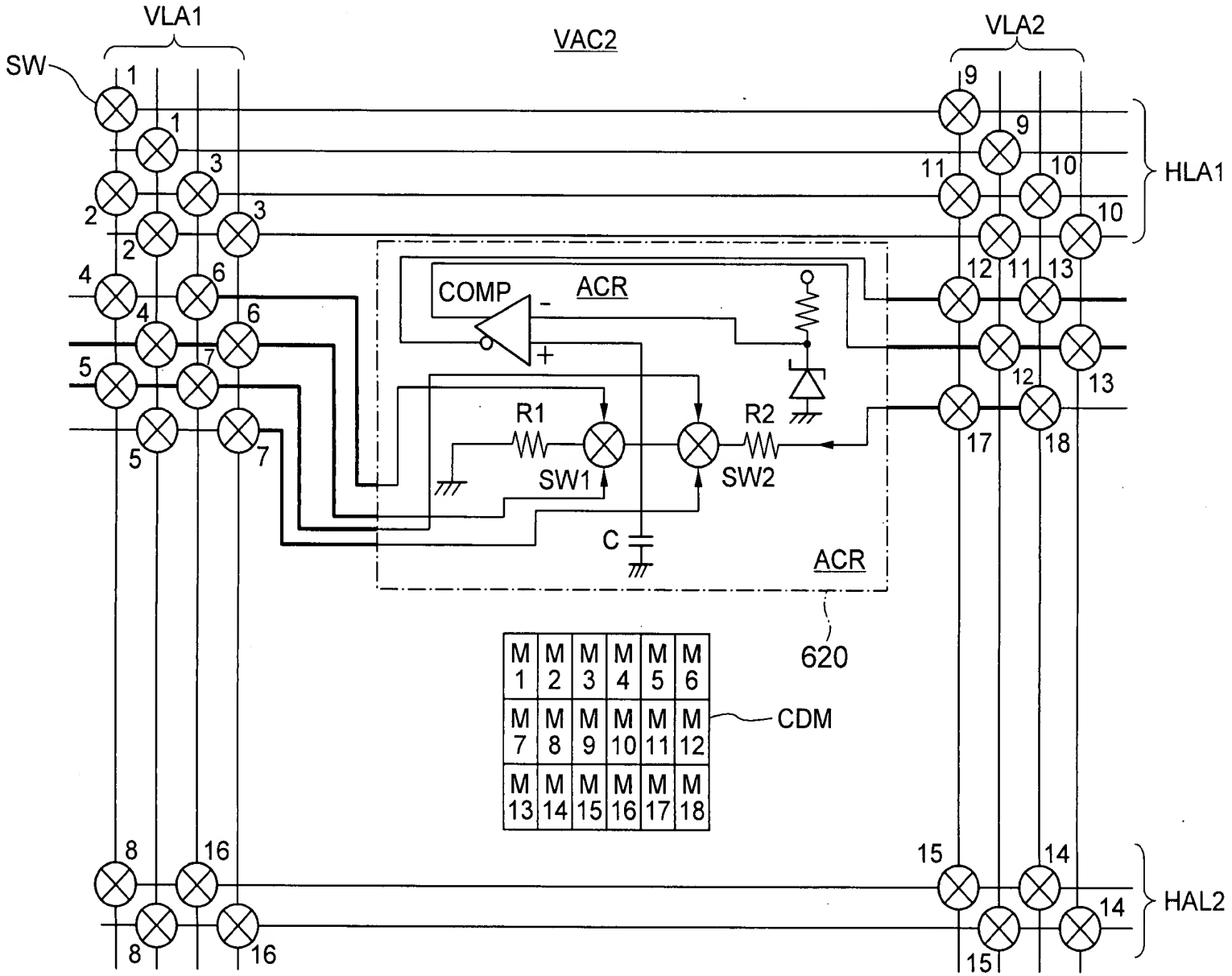

VLA1
VAC2
VLA2
SW
HLA1
COMP
ACR
R1
R2
SW1
SW2
C
ACR
620
M1 M2 M3 M4 M5 M6
M7 M8 M9 M10 M11 M12
M13 M14 M15 M16 M17 M18
CDM
HAL2

FIG. 17

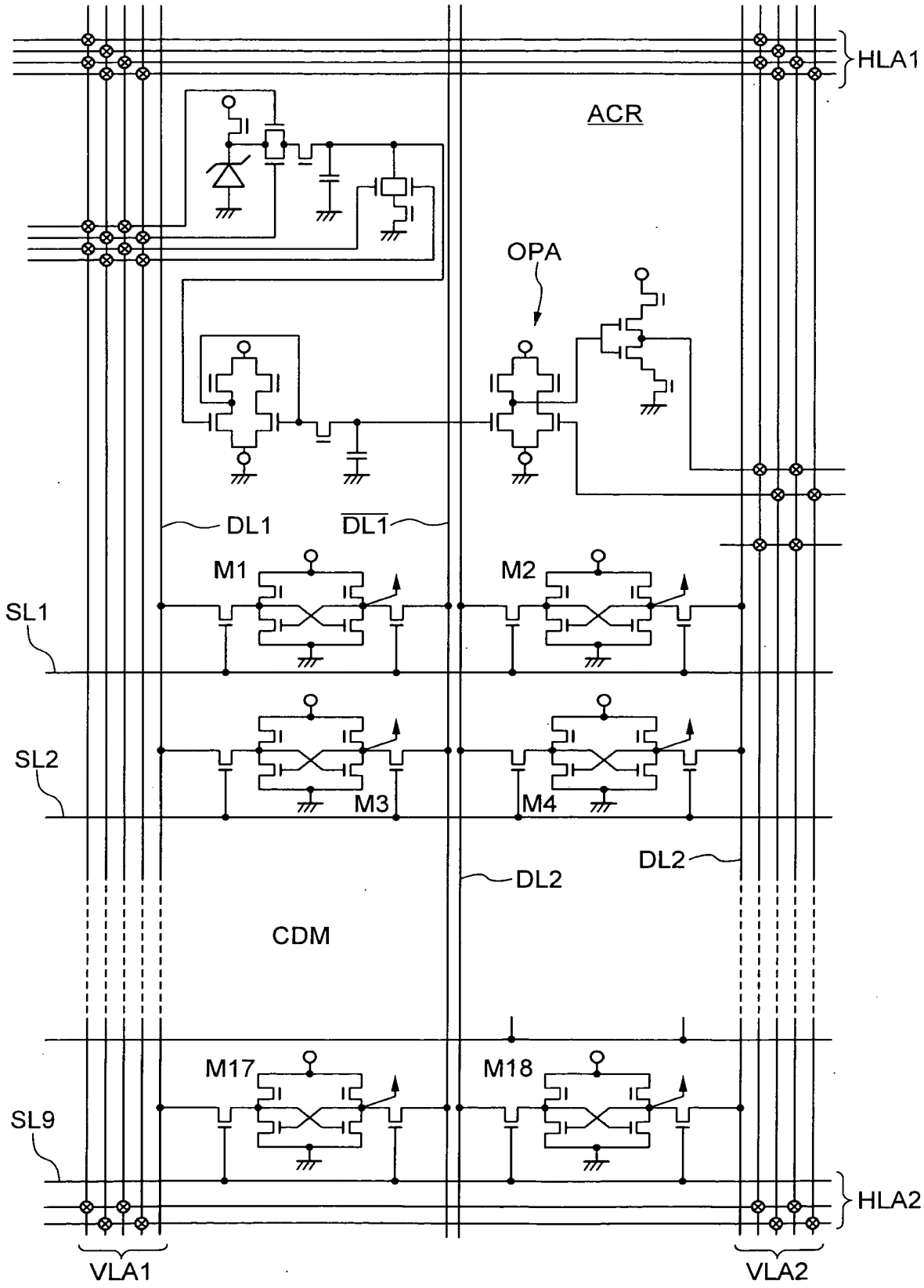

HLA1
ACR
OPA
DL1
DL1
M1
M2
SL1
SL2
M3
M4
DL2
DL2
CDM
M17
M18
SL9
HLA2
VLA1
VLA2

FIG. 18

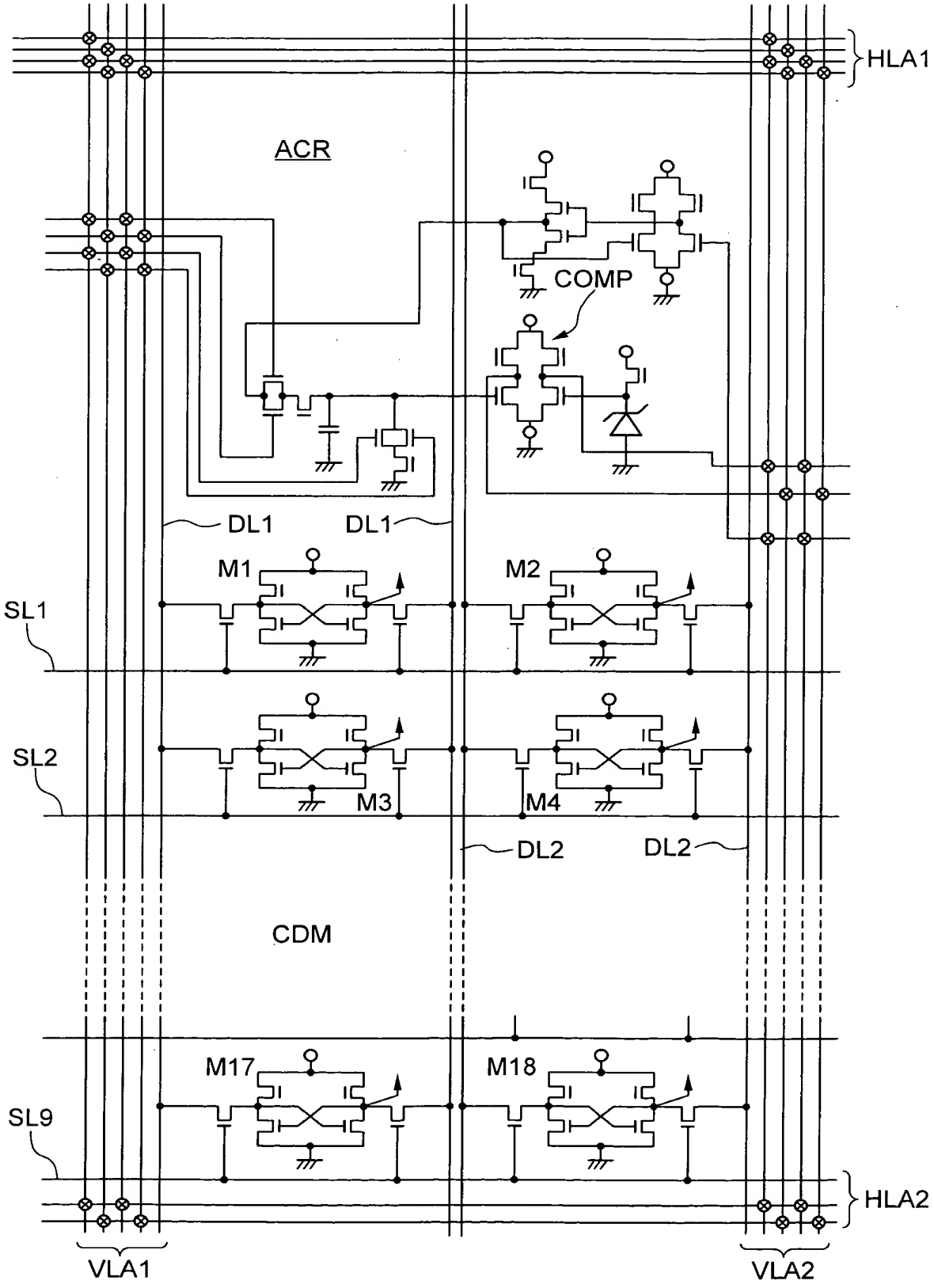

HLA1
ACR
COMP
DL1
DL1
M1
M2
SL1
SL2
M3
M4
DL2
DL2
CDM
M17
M18
SL9
HLA2
VLA1
VLA2

FIG. 19

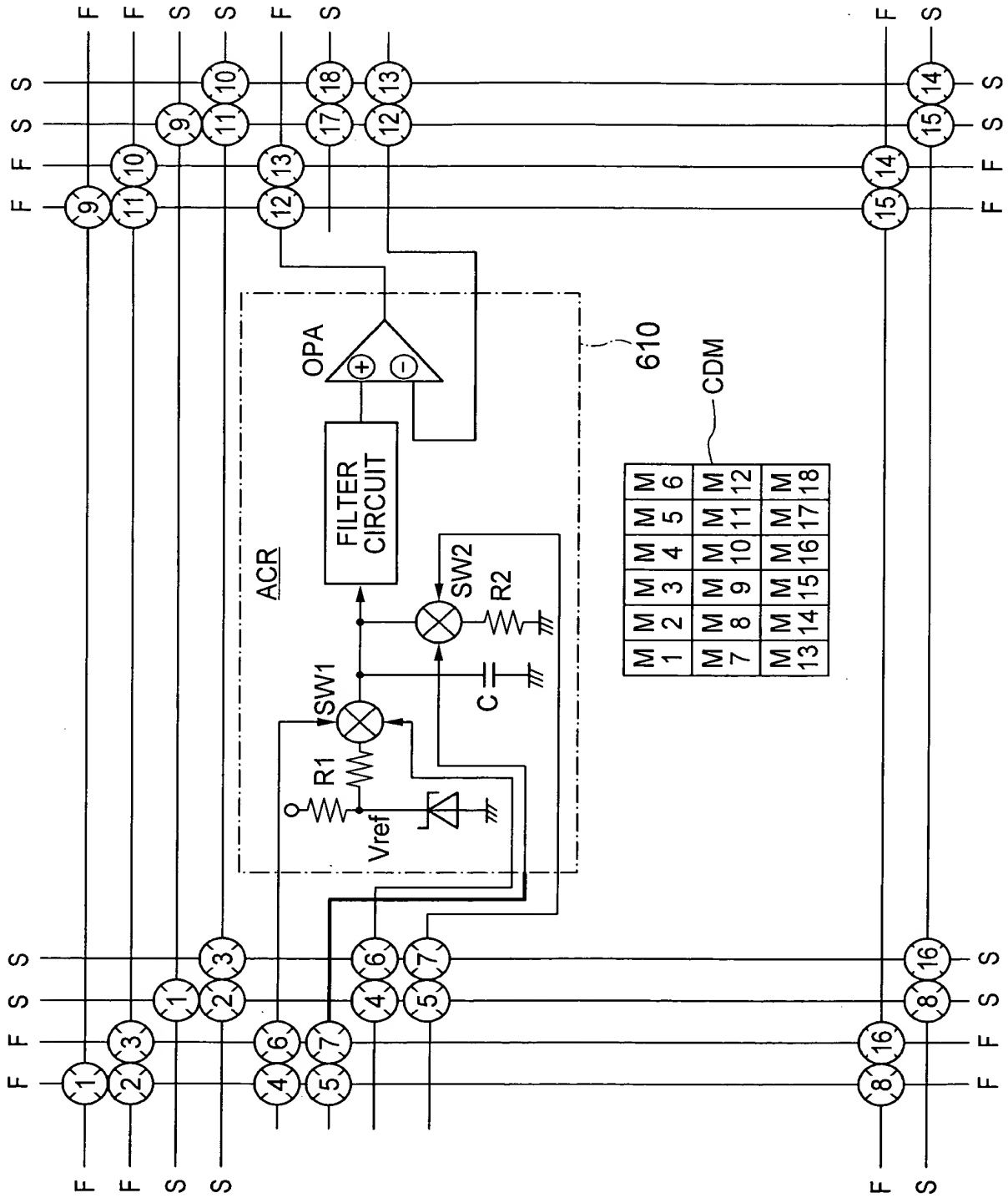

F F S S F S
F F S S F S
F F S S F S
F F S S F S
610
OPA
FILTER CIRCUIT
ACR
SW1
SW2
R1
R2
C
Vref
CDM
M 1 2 3 4 5 6
M 7 8 9 10 11 12
M 13 14 15 16 17 18

FIG. 20

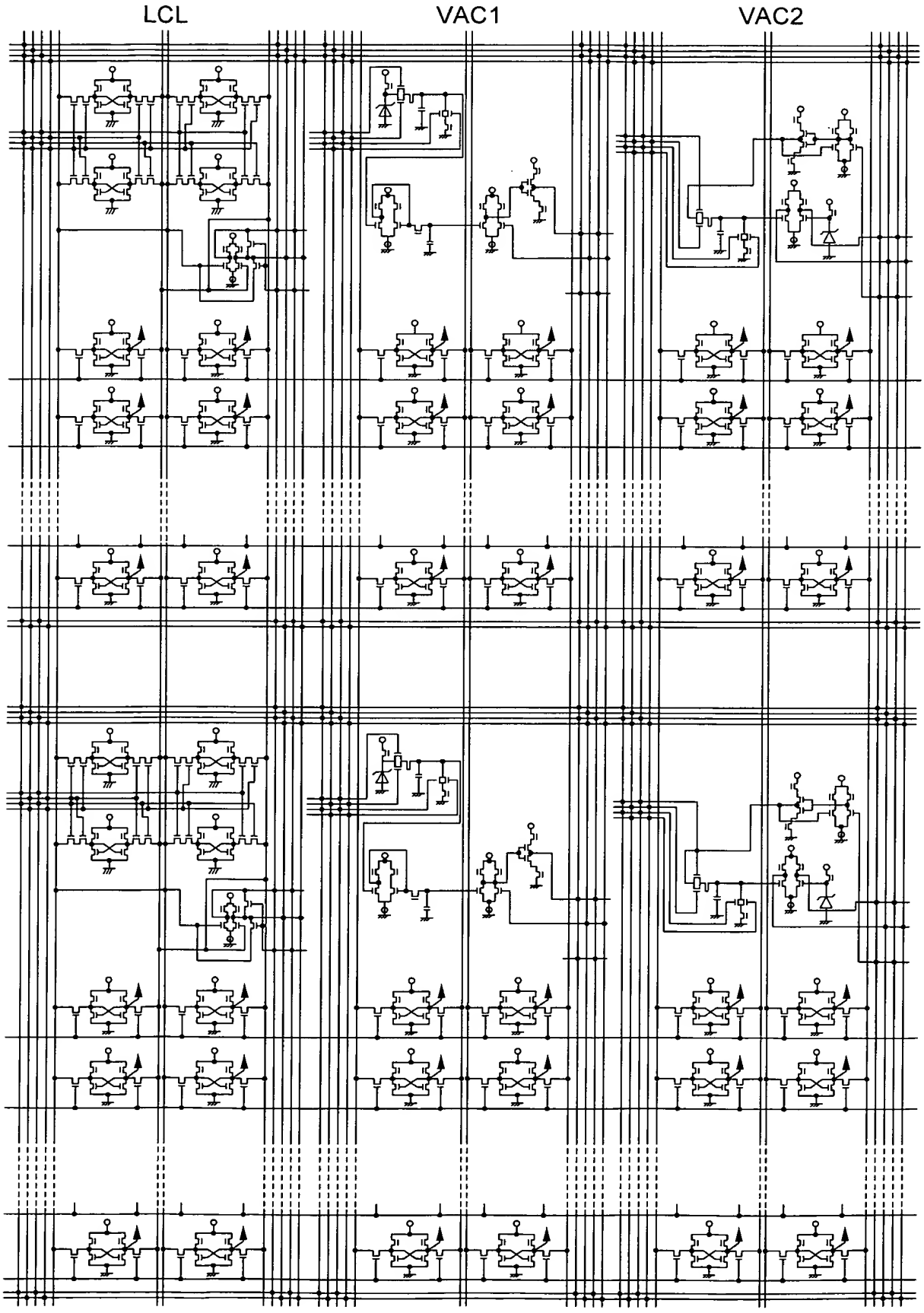


FIG. 21

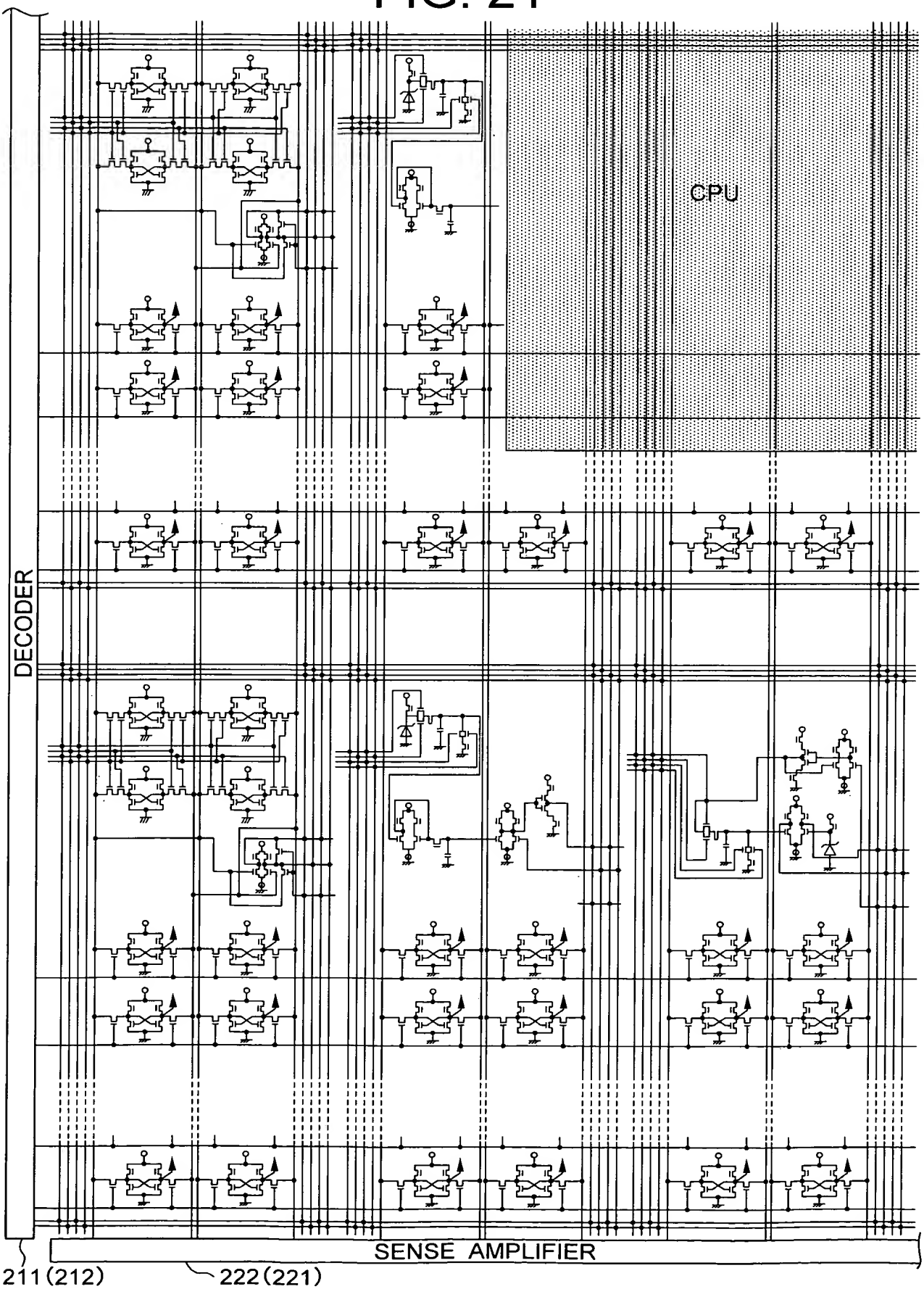


FIG. 22

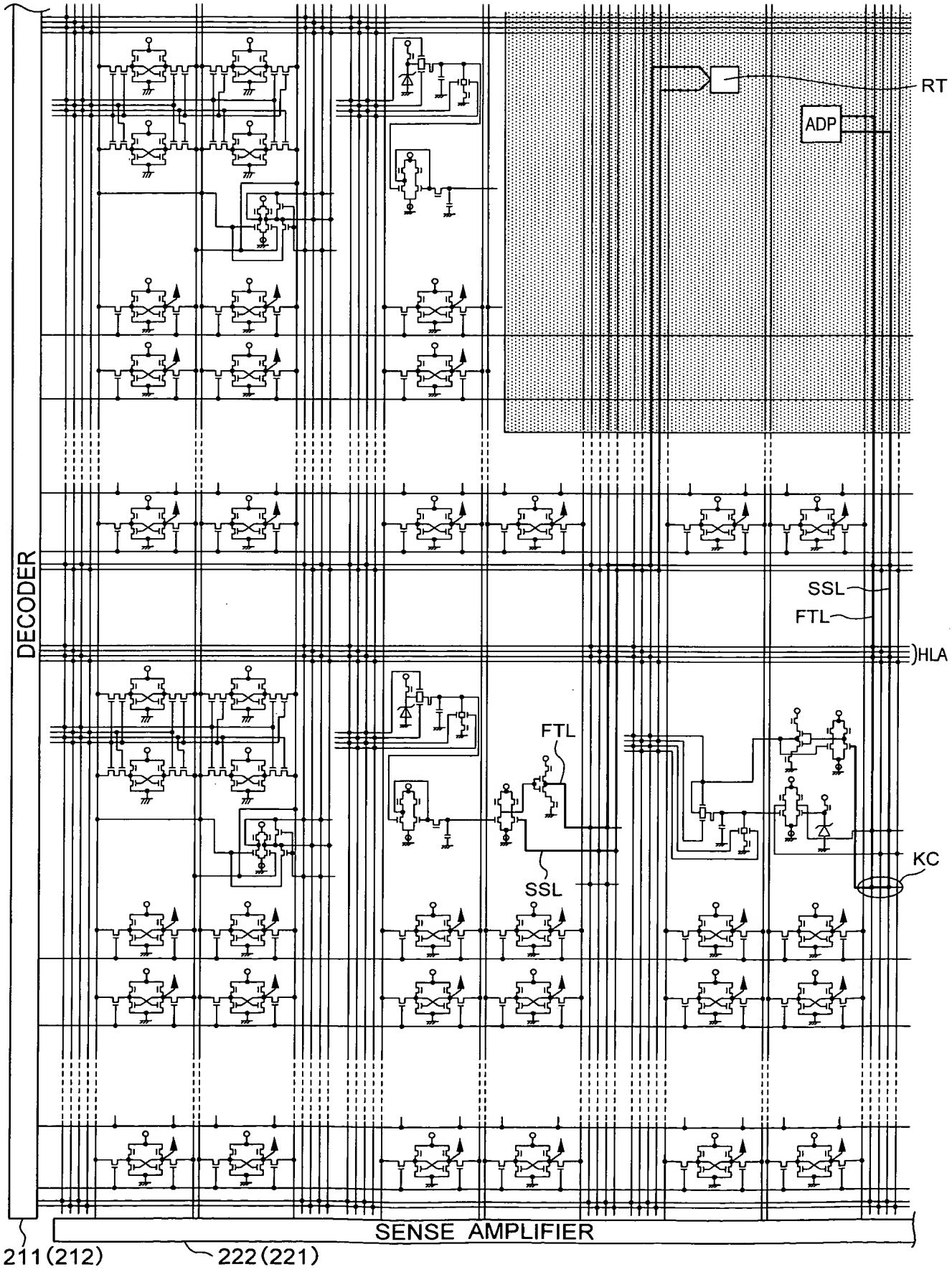

RT
ADP
DECODER
SSL
FTL
HLA
FTL
SSL
KC
SENSE AMPLIFIER
211(212)
222(221)

FIG. 23

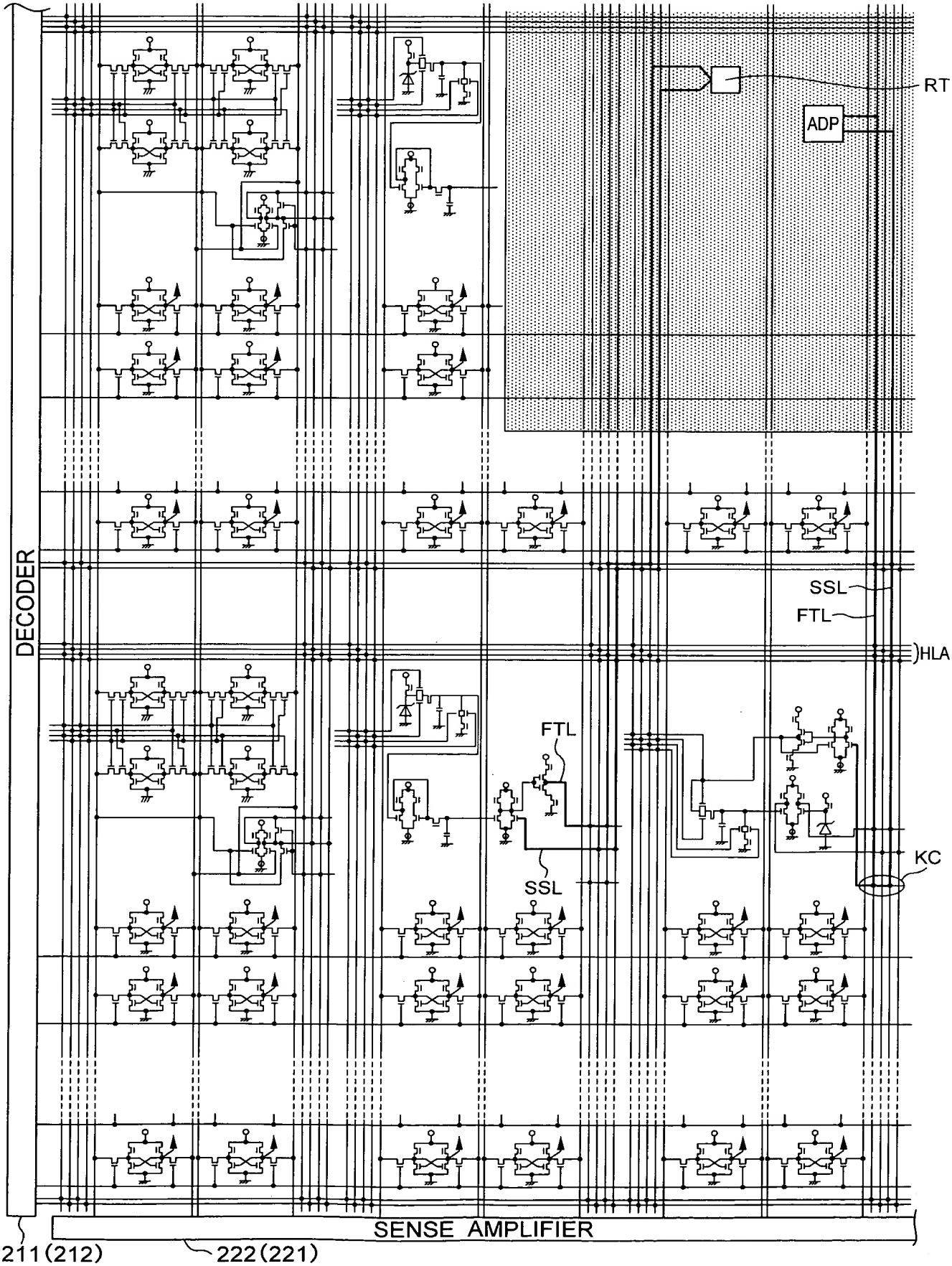

RT
ADP
DECODER
SSL
FTL
HLA
FTL
SSL
KC
SENSE AMPLIFIER
211(212)
222(221)

FIG. 24

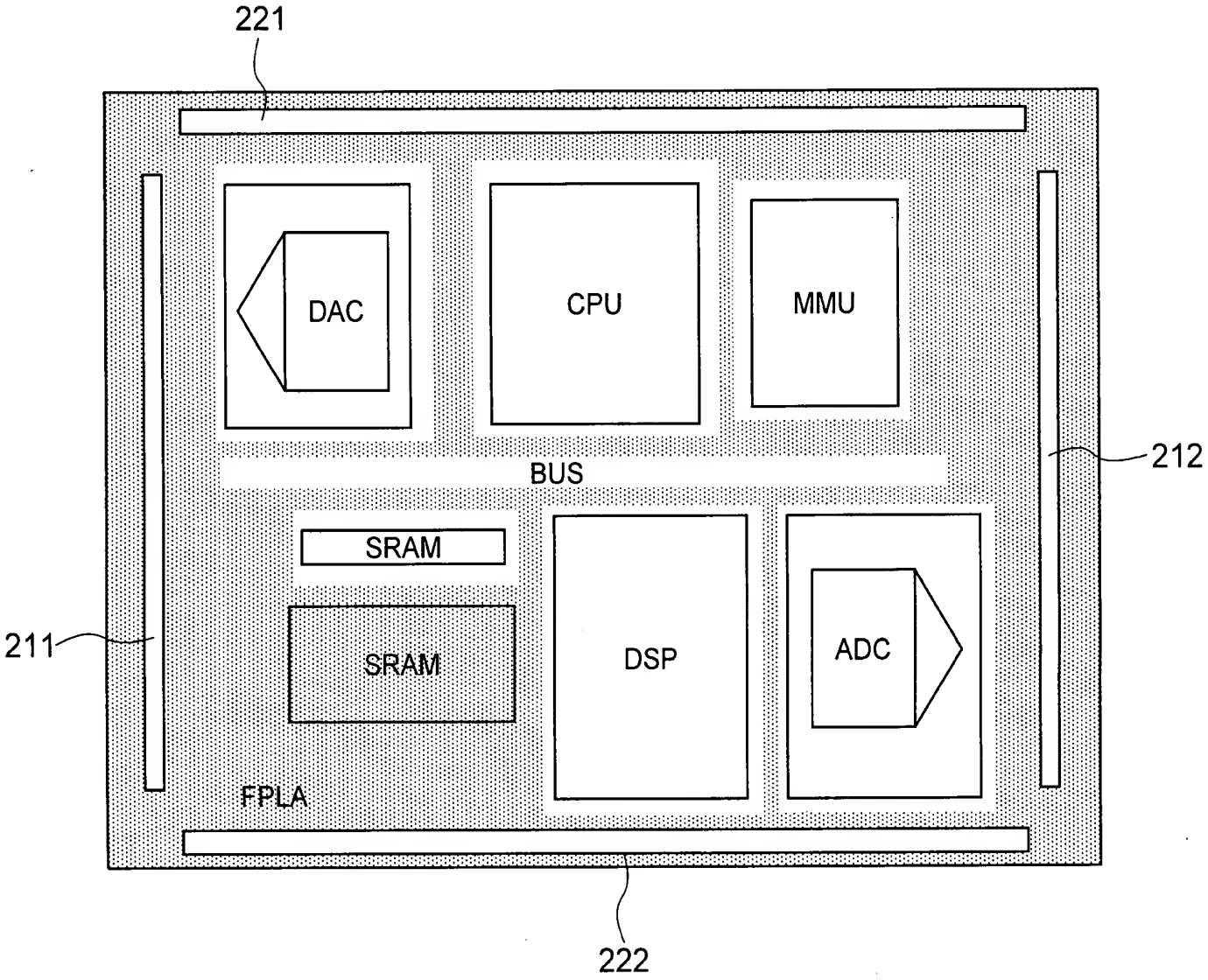


FIG. 25

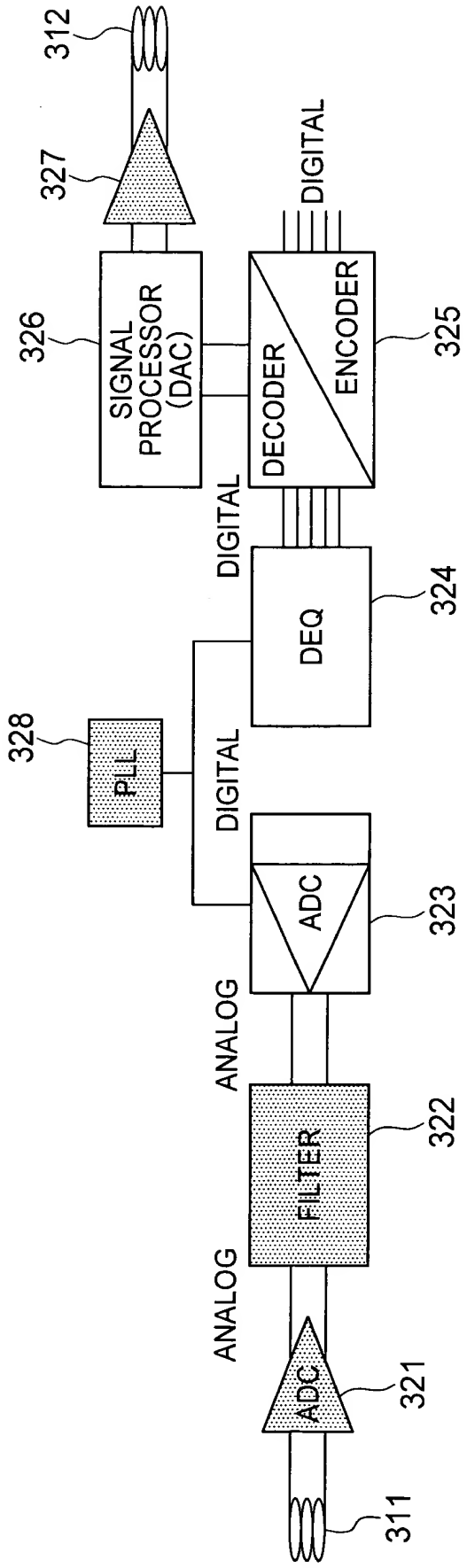

312
327
326
SIGNAL PROCESSOR (DAC)
DIGITAL
DECODER
ENCODER
325
DIGITAL
328
PLL
DIGITAL
DEQ
324
ADC
323
ANALOG
FILTER
322
ANALOG
ADC
321
311

FIG. 26

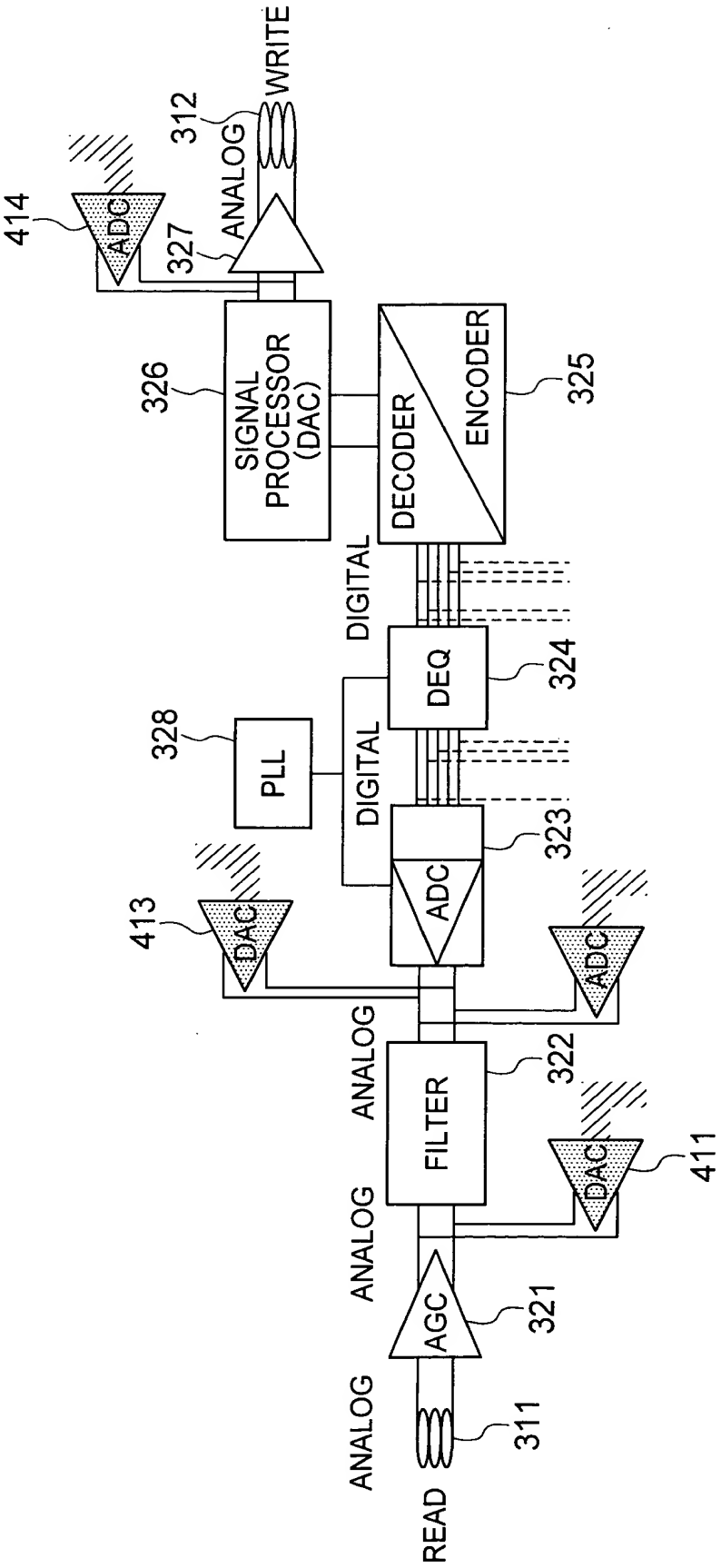


FIG. 27